

**AMENDMENTS TO THE CLAIMS:**

1-4. (Canceled)

5. (Previously presented) A group III nitride compound semiconductor device comprising:  
a substrate on which a first environment division and a second environment division are formed; and

a plurality of first group III nitride compound semiconductor layers formed on said first environment division so as to serve as effective semiconductor layers,  
wherein said first environment division comprises an outer shape having rounded corners.

6. (Previously presented) A device according to claim 5, wherein said first group III nitride compound semiconductor layers are formed on said first environment division on an exposed surface of said substrate.

7. (Previously presented) A device according to claim 6, wherein said second environment division comprises a material which prevents said group III nitride compound semiconductors from being grown on said material.

8. (Previously presented) A device according to claim 6, further comprising:  
a second group III nitride compound semiconductor layer, which is at least one of amorphous and different in crystallinity from said first group III nitride compound semiconductor layers, grown on said second environment division.

9. (Previously presented) A semiconductor device structure having a first portion and a plurality of second portions, said structure comprising:  
a substrate; and  
a separating layer formed over said substrate and defining a plurality of openings

respectively formed in said plurality of second portions,  
wherein at least one opening in said plurality of openings comprises a rounded shape.

10. (Previously presented) The structure according to claim 9, wherein said shape comprises one of a square and a rectangle, said shape having a side with a length in a range from 100 to 1000 $\mu\text{m}$ .

11. (Previously presented) The structure according to claim 9, wherein said shape comprises one of a square and a rectangle, said shape having a side with a length in a range from 200 to 800 $\mu\text{m}$ .

12. (Previously presented) The structure according to claim 9, wherein said separating layer has a thickness of about 5.5  $\mu\text{m}$ .

13. (Previously presented) The structure according to claim 9, wherein a distance between adjacent ones of said openings is about 50  $\mu\text{m}$ .

14. (Previously presented) The structure according to claim 9, further comprising:  
an undercoat layer comprising one of a metal and a metal nitride formed over said substrate in said plurality of openings.

15. (Previously presented) The structure according to claim 9, wherein each opening of said plurality of openings has a rounded shape.

16. (Previously presented) The structure according to claim 9, wherein said separating layer is formed directly on said substrate.

17. (Previously presented) A method of forming a semiconductor device structure having a

first portion and a plurality of second portions, said method comprising:

- forming a separating layer over a substrate;
- forming a mask over said separating layer;
- etching said separating layer using said mask to create a plurality of openings in said separating layer; and
- rounding at least one opening in said plurality of openings such that said at least one opening has a rounded shape.

18. (Previously presented) The method according to claim 17, wherein said forming said separating layer over said substrate comprises forming said separating layer directly on said substrate, and

wherein said forming said mask over said separating layer comprises forming said mask directly on said separating layer.

19. (Previously presented) The structure according to claim 9, wherein said separating layer comprises a material which inhibits a group III nitride compound semiconductor layer from being grown thereon.

20. (Previously presented) The structure according to claim 9, wherein said separating layer comprises one of a nitride and an oxide.

21. (Previously presented) The structure according to claim 20, wherein said nitride comprises one of BN, TiN, VN, CrN, ZrN, NbN, HfN, and TaN, and said oxide comprises one of TiO, VO, CrO, ZrO, and TaO.

22. (Previously presented) The structure according to claim 9, wherein said substrate comprises one of sapphire, silicon, silicon carbide, zinc oxide, gallium phosphide, gallium arsenide, magnesium oxide and manganese oxide.

23. (Previously presented) The structure according to claim 9, wherein said rounded shape comprises one of a square having rounded corners and a rectangle having rounded corners.

24. (Currently amended) A method of forming a group III nitride compound semiconductor device, said method comprising:

forming amorphous portions of a plurality of ion-implanted regions in a substrate surface in a grid-shaped grid-like pattern by implanting ions in said substrate surface, ~~to generate a plurality of non-ion-implanted regions of said substrate which are separated by said plurality of ion-implanted regions; and~~

forming a group III nitride compound semiconductor layer on said substrate surface such that a portion of said layer formed on said amorphous portions of said substrate surface ~~plurality of non-ion-implanted regions~~ has a different crystalline structure than a portion of said layer formed on portions of said substrate surface that are other than said amorphous portions ~~said plurality of ion-implanted regions~~.

25. (New) The method according to claim 24, wherein said portions of said substrate surface that are other than said amorphous portions comprise square-shaped portions formed between said amorphous portions having said grid-shaped pattern.

26. (New) The method according to claim 24, wherein said portion of said group III nitride compound semiconductor layer formed on said amorphous portions of said substrate surface comprises a columnarly grown portion.

27. (New) The method according to claim 24, wherein said portion of said group III nitride compound semiconductor layer formed on said amorphous portions of said substrate surface is not connected to a portion of said layer formed on said portions of said substrate surface that are other than said amorphous portions.